IN THE CLAIMS

1-163 (Canceled).

164. (Currently Amended) A fabricating method comprising the steps of:

processing semiconductor wafers by a plurality of processing apparatuses each including at least one processing chamber and an interface having transporting means for transporting a semiconductor wafer to be processed into said processing chamber and for sending out a processed semiconductor wafer~~, wherein timings of transporting the semiconductor wafers at said interfaces of said processing apparatuses are scheduled according to a predetermined scheduling, and said predetermined scheduling is made by use of a unit time which is common to all of said plurality of processing apparatuses~~; and

transporting semiconductor wafers from one of the processing apparatuses to another by an inter-apparatus transporter;

wherein, in each of said plurality of processing apparatuses, semiconductor wafers are set at said interface by said inter-apparatus transporter, transported into said processing chamber by said transporting means, processed in said processing chamber, and transported out of said processing chamber by said transporting means; and

wherein a time interval assigned ~~to~~ for transporting the semiconductor wafers from one of said processing apparatuses to another by said inter-apparatus transporter and assigned for processing in each of said processing apparatuses including time for transporting a semiconductor wafer to be processed into said processing chamber at said interface, time for processing the semiconductor wafer in said processing chamber, and time for transporting the semiconductor wafer out of said processing chamber and sending out at said interface is set ~~a~~ to N multiplication of ~~said~~ a predetermined unit time, with N being a positive integer, that is common to all of said plurality of the processing apparatuses and the inter-apparatus transporter and that is longer than the shortest required time for either processing in each of the processing apparatuses or for transporting by the inter-apparatus

transporter but shorter than the longest required time for either processing in each of the processing apparatuses or for transporting by the inter-apparatus transporter.

165. (New) A fabricating method according to claim 164, wherein said time interval assigned for processing in each of said processing apparatuses further includes time for waiting prior to transporting the semiconductor wafer to be processed into said processing chamber at said interface.

166. (New) A fabricating method according to claim 164, wherein said time interval assigned for processing in each of said processing apparatuses further includes time for waiting prior to sending out the semiconductor wafer at said interface.

167. (New) A fabricating method according to claim 165, wherein said time interval assigned for processing in each of said processing apparatuses further includes time for waiting prior to sending out the semiconductor wafer at said interface.

168. (New) A fabricating method comprising the steps of:

processing semiconductor wafers by a plurality of processing apparatuses each including at least one processing chamber and an interface having transporting means for transporting a semiconductor wafer to be processed into said processing chamber and for sending out a processed semiconductor wafer; and

transporting semiconductor wafers from one of the processing apparatuses to another by an inter-apparatus transporter;

wherein, in each of said plurality of processing apparatuses, semiconductor wafers are set at said interface by said inter-apparatus transporter, transported into said processing chamber by said transporting means, processed in said processing chamber, and transported out of said processing chamber by said transporting means; and

wherein a plurality of time intervals assigned to said processing apparatuses each including time for transporting a semiconductor wafer to be processed into said processing chamber at said interface, time for processing the

semiconductor wafer in said processing chamber, and time for transporting the semiconductor wafer out of said processing chamber and sending out at said interface are set to N multiplication of a predetermined unit time that is common to all of said plurality of the processing apparatuses with N being a positive integer, and that is longer than the shortest required time for processing the semiconductor wafer in each of the processing chambers but shorter than the longest required time for processing in each of the processing apparatuses; and

wherein a time interval assigned to transporting the semiconductor wafers from one of said processing apparatuses to another by said inter-apparatus transporter is scheduled by use of one of said time intervals.

169. (New) A fabricating method comprising the steps of:

processing semiconductor wafers by a plurality of processing apparatuses each including at least one processing chamber and an interface having transporting means for transporting a semiconductor wafer to be processed into said

processing chamber and for sending out a processed semiconductor wafer; and

transporting semiconductor wafers from one of the processing apparatuses to another by an inter-apparatus transporter;

wherein, in each of said plurality of processing apparatuses, semiconductor wafers are set at said interface by said inter-apparatus transporter, transported into said processing chamber by said transporting means, processed in said processing chamber, and transported out of said processing chamber by said transporting means; and

wherein a time interval assigned to each of said processing apparatuses including time for transporting a semiconductor wafer to be processed into said processing chamber at said interface, time for processing the semiconductor wafer in said processing chamber, and time for transporting the semiconductor wafer out of said processing chamber and sending out the semiconductor wafer to said inter-apparatus transporter at said interface is set to N multiplication of a predetermined unit time that is common to all of said plurality of the processing apparatuses, with N

being a positive integer, and that is longer than the shortest required time for either processing in each of the processing chambers or for transporting by the inter-apparatus transporter but shorter than the longest required time for either processing in each of the processing apparatuses or for transporting by the inter-apparatus transporter;

wherein a time interval between setting of a semiconductor wafer at the interface of one of said processing apparatuses by said inter-apparatus transporter and setting at the interface of another processing apparatus by said inter-apparatus transporter is set to M multiplication of said predetermined unit time, with M being a positive integer.